Large Suspended Inductors on Silicon and Their Use in a 2-μm CMOS RF Amplifier

J. Y.-C. Chang, *Student Member, IEEE,* Asad A. Abidi, *Member, IEEE,* and Michael Gaitan, *Member, IEEE*

Abstract—**Large spiral inductors encased in oxide over silicon are shown to operate beyond the UHF band when the capacitance and loss resistance are dramatically reduced by selective removal of the underlying substrate. Using a 100-nH inductor whose self-resonance lies at 3 GHz, a balanced tuned amplifier with a gain of 14 dB centered at 770 MHz has been implemented in a standard digital 2-μm CMOS IC process. The core amplifier noise figure is 6 dB, and the power dissipation is 7 mW from a 3-V supply.**

I. Introduction

THE growing needs for miniature wireless communication in the 1-GHz band have prompted interest in monolithic RF amplifiers in silicon. Modern bipolar transistors and FET's certainly have a high enough f_T to provide gain in the required narrow frequency band at these frequencies; the challenge, interestingly enough, is in the difficult fabrication of monolithic passive components. An RF amplifier employs a tuned load, to act as a secondary filter for out of band signals and noise following preselection at the antenna, but most importantly as a means to obtain gain which may be as large as that available at dc by using LC resonance to null out device and parasitic capacitances at the center frequency.

Efforts to fabricate large value spiral inductors on silicon substrates in the 1960's [1] led to the conclusion that the self-resonance caused by parasitic capacitance of these structures to the substrate would limit their use at high frequencies, and the series spreading resistance in the lossy substrate their quality factor (Q). Spiral inductors were revisited when the fabrication of tuned amplifiers became common on the semi-insulating GaAs substrate, where these limitations no longer exist. Most GaAs circuits required inductances of only a few nanohenries.

The work reported here was motivated by the need to develop a silicon *low-power* RF amplifier in the 800- to 900-MHz frequency band. A low-power amplifier must necessarily operate at a high impedance level, and therefore requires large inductors in the tuned load. Previous work [2] in a 0.3-μm GaAs MESFET technology has demonstrated a monolithic RF amplifier tuned to 1.6 GHz with a conventional on-chip inductor of about 12 nH. We set ourselves the greater challenge of obtaining a similar performance in the 700- to 900-MHz band with a 2-μm digital silicon CMOS technology. The lower frequency of operation means that the tuned load requires inductors as large as 100 nH. Lessons learned from past efforts in inductor fabrication on silicon suggested, however, that, short of a fundamental innovation, this was an impossible goal. How this challenge was met is described in the following sections.

Manuscript received February 12, 1993. This work was supported by DARPA, Rockwell International, and the State of California MICRO Program. In this report, commercial computer programs and instruments are identified to specify the procedure adequately. This does not imply recommendation or endorsement by NIST, nor that the program is the best available for the purpose.

J. Y.-C. Chang and A. A. Abidi are with the Integrated Circuits and Systems Laboratory, Electrical Engineering Department, University of California, Los Angeles, CA 90024-1594.

M. Gaitan is with the Device Technology Group, Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD 20899.

IEEE Log Number 9208809.

II. A Suspended Inductor

Large-value inductors may be fabricated as aluminum spirals with many turns. As the inductance of the spiral is made larger, the capacitance to substrate increases, leading to a progressively *lower* frequency of self-resonance. Spiral inductors of 25 nH are found to self resonate at about 3 GHz on GaAs substrates [2] and on insulating sapphire substrates [3]. On the other hand, aluminum inductors only as large as 10 nH on standard silicon substrates will self resonate at 2 GHz [4], and furthermore the spreading resistance of the substrate will introduce a loss.

These characteristic problems of a silicon substrate may be overcome if the area under the inductor is made to appear locally insulating. This is most simply accomplished by selectively etching out the silicon, leaving the inductor encased in a suspended oxide layer attached at four corners to the rest of the silicon IC. There is a similarity between this technique and the practice in some GaAs technologies of suspending spiral inductors on air bridges [5], but as the typical gap under an air bridge is 3 μm, while removal of the substrate offers air gaps as large as 200 to 500 μm, inductors fabricated by our technique obtain a much lower capacitance to substrate.

A 100-nH inductor was designed using analytical formulas [6] as a 20-turn square spiral of 4-μm-wide lines of second-layer aluminum metal separated by 4-μm spaces, resulting in an outer dimension of 440 μm. Simulations on the SONNET® EM 3-D electromagnetic simulator showed that removal of the underlying substrate will cause the inductor self-resonance to move out from 800 MHz to 3 GHz (Fig. 1).

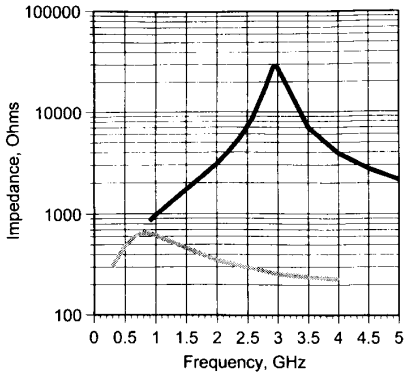

Fig. 1. Self-resonance frequency of a 100-nH inductor increases from 800 MHz to 3 GHz after removal of underlying substrate. This corresponds to a 14-fold reduction in parasitic capacitance. Impedance of inductor over silicon (gray) and over pit (black) obtained from 3-D electromagnetic simulations.

Accompanied by active circuits for an amplifier and buffers, this structure was fabricated through MOSIS as a standard n-well 2-μm CMOS IC. Using a previously described technique [7], the fabricated die were then subject to a selective EDP wet etch to remove the substrate under the inductors, while leaving the remaining circuits intact (Fig. 2). The starting areas for the etch were defined without use of an extra mask [7].

III. RF Amplifier and Experimental Results

Two identical inductors of nominal value 100 nH were used as the load of a balanced amplifier, tuned to a center frequency of 800 MHz by the junction capacitance of FET's built with 2-μm design rules (Fig. 3). The circuit attained high-frequency gain at low power at the expense of noise figure. Cascode stages were used to enhance the available gain. For ease of testing in a network analyzer, on-chip polysilicon 50-Ω resistors terminated the two inputs to ground. The outputs were buffered through common-source FET's to a 50-Ω environment off-chip. The buffer frequency response was separately measured to deembed the core amplifier.

Operating at a 3-V power supply, a peak gain of 14 dB centered at 770 MHz was obtained in the core amplifier with a 7-mW power dissipation. The measured frequency response conformed well to simulations (Fig. 4), although the center frequency was lower by 50 MHz owing to a larger FET junction capacitance than anticipated. Chips where the substrate was left intact under the inductor show a dramatically worse frequency response (Fig. 4). The measured noise figure of the core amplifier, excluding the noise contribution of the termination resistors, was 6 dB. As the substrate capacitance and loss in the suspended inductor are negligibly small, it was modeled for the purpose of circuit simulation by a simple *LCR* equivalent circuit, whose parameter values correspond very well to Cascade® probe measurements on a test inductor (Fig. 4). The large suspended structure is found to be mechanically very robust. No damage has yet been observed on an IC when it sustained impacts during the packaging procedure and while measurements were being taken.

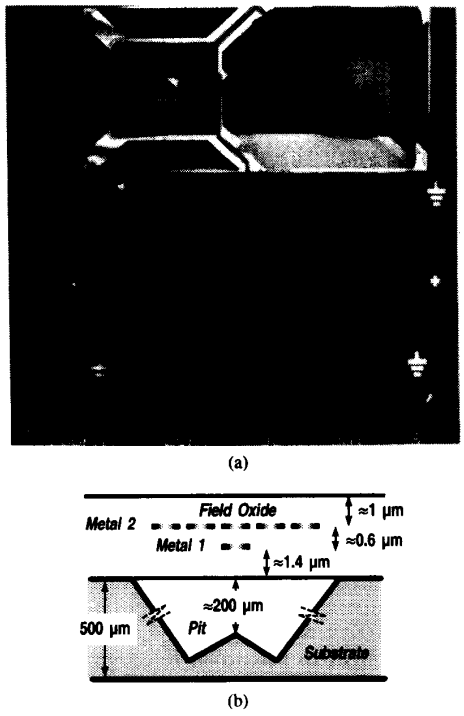

Fig. 2. (a) SEM of RF amplifier after selective substrate etch. Inductor shown is suspended on oxide layer attached to substrate at four corners. Spiral fabricated as second-level aluminum, while contact from center brought out on first level. Second inductor has been manually removed to show pit. (b) Cross section of suspended inductor and substrate after etching.

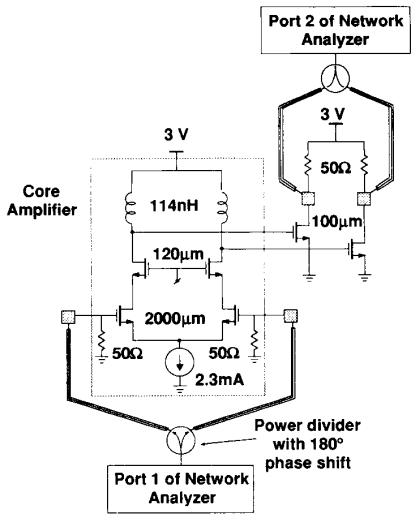

Fig. 3. Schematic of CMOS RF amplifier, including test arrangement. All FET's are 2-μm channel length. Bond pads define the chip periphery.

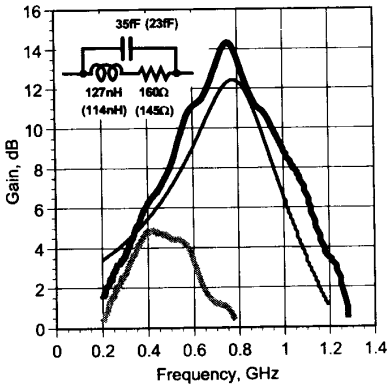

Fig. 4. Measured frequency response of core amplifier, after (black) and before (gray) substrate removal. Simulated response from SPICE (thin black) using a two-terminal *LCR* inductor model obtained from EM simulations. Measured parameter values in equivalent circuit (inset) compare favorably with values obtained from 3-D simulations (in parentheses).

IV. Conclusions

A use of selective etching is shown to obviate problems which were thought to plague all selective RF circuits on silicon substrates. As an added bonus, the etching requires no modifications to a standard digital CMOS IC process. The test vehicle is possibly the highest performance 2-μm CMOS amplifier reported to date, with a 14-dB gain at 770 MHz while requiring only a 3-V power supply from which it drains 7 mW.

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